EE/CprE/Se 491 Weekly Report X
10/11/24 - 10/17/24
sdmay25-28
Digital ASIC fabrication
Client & Advisor: Dr. Duwe

Team Members
Calvin Smith – Issue Tracking
Camden Fergen - Testing Lead
John - Team organizer
Nicholas - Verilog Lead
Levi - Client interaction

Weekly Summary

This past week we worked on researching CGRAs, looking at chip generators like RocketChip and Litex, and working on getting the VM setup. This came from the meeting with professor Duwe where he gave us guidance on what we should be researching and what we should be using. We performed various other tasks like updating a Gantt chart and updating our planned tasks.

Pask Week Accomplishments

- Calvin:
    - Created Presentation for advisor meeting
    - Explored and discussed various options for hardware design language
    - Researched Litex chips for use as a base model
    - Scrapped current rocketchip toolchain due to concerns regarding chisel
- Camden:
    - Started to get VM software setup and installed
    - Worked to get project planning corrected and try to plan the next month
    - Updated Gantt chart to accurately reflect team work recently
    - Lead team planning meeting
- John:
    - Worked with caravel and Efabless
    - Continued research with RISC-V
    - Researched CGRAs and their implementations
    - Worked on PowerPoint for Duwe presentation
- Levi:
    - CGRA research

- Nicholas:
    - Started working on a RISC ALU in verilog
        - Completed AddSub unit and various Logical units.
    - Create SRAM using OpenRam.
    - Started looking into implementing a CGRA
    - Looked at team Dec24-12s (including multiple projects on one Digital ASIC) project to see how our basic ALU would be implemented into their design.

Name	Individual Contribution	Hours this Week	Hours Cumulative
Calvin	-Litex cpu research -Rocket Chip toolchain exploration -Advisor meeting discussion lead -Advisor meeting presentation	6.001	28.923
Camden	• Started setting up VMs for team development • Work on lightning talks and design documentation • Headed meeting with project planning and tracking	6	30
John	-Worked with caravel and Efabless -Continued research with RISC-V -Researched CGRAs and their implementations - Worked on PowerPoint for Duwe presentation	6	30
Levi	-CGRA research	6	30
Nicholas	-RISC ALU work -SRAM creation -CGRA research	8	34

Plans for Upcoming Week

- Calvin:
    - Get the Litex toolchain up and running on the VM
    - Isolate ALU from Litex core to compare for use against an adapted MIPS ALU
    - Fun verilog learning time
- Camden:
    - Continue getting VM setup, contact Gregory from chipforge to get anything installed that is needed for efabless
    - Contact etg to get Vivado and questasim installed on the VM as they require special installs
- John:
    - Help Nicholas with working on the SRAM and ALU
    - Work with verilog and efabless
    - Research differences between RISC-V and MIPS architectures and find how they affect the ALU
- Levi:
    - Get familiarized with VMs
    - CGRA implementation in verilog
- Nicholas:
    - Use SRAM to recreate datapath two of CprE 381 and Harden completed project.
    - Write a primitive CGRA circuit in verilog.
    - Complete Barrel Shifter for ALU.

Summary of weekly advisor meeting

This week we spoke with Duwe about using an FPGA fabric, but he mentioned not thinking about it as an FPGA but more like a programmable accelerator and that we should research CGRAs and how they can relate to our project. Work on documentation as this will be an educational piece for ChipForge members. We also should be finding applications, currently our possible applications consist of an eINK display and AI models. Duwe also mentioned that we should use something like RocketChip or Litex to make development faster so that we don't need to develop from scratch.